: Design of next-generation Tb/s turbo codes

This PhD thesis aims at investigating Forward Error Correcting (FEC) codes of the turbo family, able to achieve or approach Tb/s decoding throughputs. The thesis will focus on the study of architecture-aware encoding, puncturing and decoding algorithms as well as of the corresponding architecture templates. Several turbo code structures will be investigated, namely conventional and flexible-degree turbo convolutional codes.

The thesis work will be carried out in the framework of the upcoming H2020 European project EPIC (Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding, Sep. 2017 – Aug.2020). EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes to enable practical wireless Tb/s link technology—corresponding to a 10x–100x throughput improvement over the state of the art.

The thesis work will be carried out in the Electronics department of IMT Atlantique. Its research activity is mainly dedicated to the joint design of algorithms and hardware architectures (Algorithm-Silicon Interaction) for digital communication applications. Since the invention of turbo codes in the early nineties, this research team has been internationally recognized for its expertise in channel coding and iterative processing and has designed turbo codes for several 3GPP and DVB standards. The scientific work of the team has already been awarded several national and international prizes, including the 2003 IEEE Richard W. Hamming Medal, the 2005 Marconi Prize or the 2009 IEEE/SEE Glavieux Prize.

The team has been recently involved in the design of new FEC codes (turbo and turbo-like codes) for 5G within the H2020 project FANTASTIC-5G (Flexible Air iNTerfAce for Scalable service delivery wiThin wIreless Communication networks of the 5th Generation) and is currently participating in the 5G standardization in 3GPP RAN1 NR (New Radio) activities.

The thesis work will be carried out in the framework of the upcoming H2020 project EPIC (Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding, Sep. 2017 – Aug.2020). EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes to enable practical wireless Tb/s link technology—corresponding to a 10x–100x throughput improvement over the state of the art.

Efficiently achieving ultra-high throughput (up to and exceeding Tb/s) for turbo codes is very challenging, since turbo codes are inherently serial at the component decoder level (Soft-In Soft-Out decoders). This target entails constraints on the turbo encoder/decoder such as latency and energy efficiency. The following table presents various recent turbo decoder implementations that represent the state of the art options.

Turbo	[1]	18432	LTE	45	2.00	600	1.67	0.83	1500	1.25
Turbo	[2]	18432	LTE	90	19.7	625	2.27-3.3	0.12-0.17	637-438	0.073
Turbo	[3,4]	18432	LTE	65	109	410	15.8	0.145	608	0.09

Additional application-dependent constraints such as code flexibility and error rate performance should also be met. Addressing all of these constraints requires the exploration of code design, decoding algorithms and highly parallel architecture templates.

In this work, we will investigate FEC codes of the turbo family with the study of architecture-aware encoding, puncturing and decoding algorithms as well as of the corresponding architecture templates able to achieve or approach Tb/s decoding throughputs. Several turbo code structures will investigated, broadly divided into classical and flexible-degree turbo convolutional codes.

The conventional turbo code structure [5] (parallel concatenation of two recursive systematic convolutional codes) is adopted for this phase.

- : degrees of freedom for code design are solely represented by the choice of interleaving and puncturing. Exploitation of full parallelism represents the main axis of improvement for hardware implementations. However, the corresponding routing congestion represents the biggest challenge for very high throughput architectures. Enforcing regularity and locality is the most efficient way to reduce routing congestion, but code performance requires randomness from a communication point of view. Thus, this task will investigate this trade-off under DSE process in the optimization of interleaving and puncturing.
- : Joint optimization of puncturing and interleaving to improve performance of high-rate Turbo codes will be explored. Highly regular interleaving and puncturing structures by applying periodicity on the resulting jointly optimized interleaving and puncturing patterns will be developed.
- : Develop a fully parallel, pipelined architectural template for the resulting turbo codes.

:

- : a turbo code can be seen as a serial concatenation of a degree-2 repetition code, an interleaver and a convolutional code. The generalization of this structure through the variation of the repetition degrees enables a finer control over performance and complexity, and thus provides an additional degree of freedom to the DSE. This promising approach will be investigated as a means to achieve efficient high-throughput parallel decoders with an improved performance vs. complexity trade-off.
- : A new code design characterized by a flexible degree of input bits based on the structure of irregular Turbo codes where degree-1 bits are not precluded will be investigated. The extension to non-binary component convolutional codes [6,7] when associated with high order modulations will be studied.

- : A joint design of puncturing and interleaving to fully take advantage from this new structure will be derived and new puncturing and interleaving methods will be developed.
- : An architectural template which allows exploiting the flexibility feature at design time of this new type of turbo codes will be developed.

[1] G. Wang, H. Shen, Y. Sun; J. R. Cavallaro, A. Vosoughi; Y. Guo, "Parallel interleaver design for a high throughput HSPA+/LTE multi-standard turbo decoder", *IEEE Transactions on Circuits and Systems*, vol. 61, no. 5, pp. 1376 – 1389, May 2014.

[2] R. Shrestha and R. P. Paily, "High-throughput turbo decoder with parallel architecture for LTE wireless communication standards," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 9, pp. 2699-2710, Sept. 2014.

[3] R.G. Maunder, "A fully-parallel turbo decoding algorithm," *IEEE Transactions on Communications*, vol. 63, no. 8, pp. 2762-2775, Aug. 2015.

[4] Li, L. Xiang, T. Chen, R. G. Maunder, B. M. Al-Hashimi and L. Hanzo, "VLSI Implementation of Fully Parallel LTE Turbo Decoders", *IEEE Access*, vol. 4, pp. 323-346, 2016.

[5] C. Berrou, A. Glavieux and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: turbo-codes", *IEEE ICC '93*, Geneva, 1993, pp. 1064-1070.

[6] G. Liva, E. Paolini, S. Scalise, M. Chiani, "Turbo codes based on time-variant memory-1 convolutional codes over Fq," *IEEE ICC 2011*, Kyoto, June 2011.

[7] G. Liva, E. Paolini, B. Matuz, S. Scalise, and M. Chiani, "Short Turbo Codes over High Order Fields", *IEEE Transactions on Communications*, vol. 61, no. 6, pp. 2201 – 2211, June 2013.

Supervisor: Dr (charbel.abdelnour@imt-atlantique.fr)
Co-director: Prof. (Emmanuel.Boutillon@univ-ubs.fr)
Co-director: Prof. (catherine.douillard@imt-atlantique.fr)
Workplace: IMT Atlantique/Electronics Department
Lab-STICC laboratory/ IAS Team
Technopole Brest Iroise – CS 83818 – 29238 Brest Cedex 3 – France

:

- Master and/or Engineering Degree (Telecommunication Engineering, Electrical Engineering)
- Digital communications, coding theory, HW architectures
- Matlab, C/C++ programming
- Good English language proficiency

Send CV and cover letter to charbel.abdelnour@imt-atlantique.fr and catherine.douillard@imt-atlantique.fr