TITRE DE LA THESE :
EC2MEM – Advanced error correction **C**odes for **E**merging **MEM**ories

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Laboratoire(s) :

GEPEA	IRISA	**Lab-STICC**	LATIM
Lego	LEMNA	LS2N	hors Laboratoire

Equipe(s) de recherche : 2AI

Département(s) IMT Atlantique :

DAPI	DSEE		INFO	ITI	LCI	LUSSI
MEE	MO	OPT	SSG	SRCD	SUBATECH	

S'agit-il d'une thèse en cotutelle internationale ?
Oui **Non**
Si oui, organisme avec lequel la cotutelle est envisagée :
cotutuelle with University of Würzburg (Germany)

Le sujet proposé présente-il un caractère interdisciplinaire ?
Oui **Non**
Si oui, expliquer brièvement pourquoi (2 ou 3 lignes) : This PhD topic is inherently interdisciplinary, bridging together information theory, digital circuits, and memory technologies towards the joint design of new decoding codes and algorithms, explicitly taking into account the architecture and modern technologies of embedded memories.

La source du co-financement est-elle identifiée ?
Oui **Non**
Si oui, préciser quel co-financement est envisagé :
Co-funding is provided by the University of Würzburg (Germany).

Autres informations :
Informations utiles que vous souhaiteriez communiquer (si pertinent) :
We have applied for co-funding from the region of Bretagne (ARED), but since the results are not guaranteed or received yet, we are opting for this alternative funding as a backup.

Contexte ou état de l'art scientifique :

Décrire en 5 à 10 lignes le contexte de la thèse.

Improving the reliability and efficiency of memory components is key to emerging embedded applications like embedded AI for autonomous driving which should meet extremely challenging bandwidth, latency and safety requirements. For these emerging applications, spintronic post-CMOS memory devices will play a key role in shifting the paradigm towards a frugal "digital world" where energy consumption becomes a prime figure of merit.

Among the explored post-CMOS technologies are Magnetoresistive Random Access Memory (MRAM), Phase change Random Access Memory (PRAM), Resistance Random Access Memory (ReRAM) and more recently Racetrack Memory (RTM). All technologies are subject to process variations and multi-bit error events, requiring Error Correcting Codes (ECC) to meet the requirements.

Current ECC solutions targeting more conventional Non-Volatile Memories like multi-bit NAND Flash mainly rely on hard decision decoding of block codes or soft decoding of binary Low-Density Parity-Check codes. However, with the tendency to increase the density of emerging memory architectures to store multiple bits on the same memory element, powerful Non-Binary (NB) ECC are expected to bring a step-up in performance, thanks to their ability to decode/correct multiple bits together matching the memory architecture.

Objectifs de la thèse :

Décrire en 10 à 15 lignes les résultats attendus.

The EC2MEM project aims to investigate advanced ECC for emerging Non-Volatile Memories including Non-Binary Turbo Codes (NB-TCs) first proposed in 2018 at IMT Atlantique. The goal is the joint design of code and simplified decoding algorithms, explicitly considering the post-CMOS memory device properties and architecture that dictate the distribution of errors within the memory.

The main objective of the EC2MEM project is therefore to consolidate recent advancements on code design of NB codes and spintronic memory devices with emerging more conventional Non-Volatile Memories like multi-bit NAND Flash. The methodological approach is to link best practices of the three research communities in order to propose an efficient ECC tailored to the specific device characteristics of selected spintronic devices and corresponding memory architectures. This co-design approach helps to identify and mitigate bottlenecks stemming from the more complex decoding of NB codes while fully benefiting from their superior error correction. Thereby, the full potential for reduced power consumption and access latency expected from emerging spintronic memory devices is leveraged.

At the crossroad between three research communities EC2MEM aims to provide innovative solutions to problems inherent to emerging memory architectures by tailoring the ECC specifically to the characteristics of the spintronic memory devices.

Thereby it allows to sustainably include spintronics in the national electronics strategy for communication and artificial intelligence which need high bandwidth, high-capacity memory devices with low access latencies and energy consumption. EC2MEM reinforces the leadership position of IMT Atlantique (France) in the field of code- and decoding algorithm design by creating a link between the PEPR SPIN and the PEPR 5G and Future Networks.

Compétences attendues du ou de la candidat·e :

Lister les principales compétences nécessaires pour ce sujet de thèse.

The candidate must have a Master's degree or equivalent (engineer Bac+5) in telecommunications or electronics. Expected skills include:

- Solid skills in digital communications and/or digital design, in particular for channel coding.
- Mastery of simulation tools (MATLAB/Simulink) and programming (Python/C++).
- Practical experience with embedded systems, memory technologies and FPGAs.
- Ability to collaborate in a multidisciplinary and international environment.
- Communication and scientific writing skills in English.
- Ability to work in autonomy, develop innovative solutions and integrate them into practical applications.