IMT Atlantique
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AVIS DE SOUTENANCE DE THESE

DOCTORAT BRETAGNE LOIRE MATHSTIC

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Dpt ELEC (Laboratoire Lab-STICC)

Soutiendra ses travaux en vue de l'obtention du grade de

Docteur d'IMT Atlantique

Dans le cadre de la co-accréditation de thèse d'IMT Atlantique
au sein de l'école doctorale MathSTIC

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(dispositions exceptionnelles durant la crise sanitaire liée au Covid19)

New design approaches for flexible architectures and in-memory computing based on memristor technologies

Résumé :

The recent development of new non-volatile memory technologies based on the memristor concept has triggered many research efforts to explore their potential usage in different application domains. The distinctive features of memristive devices and their suitability for CMOS integration are expected to lead for novel architecture design paradigms enabling unprecedented levels of energy efficiency, density, and reconfigurability. In this context, the goal of this thesis work was to explore and introduce new memristor-based designs that combine flexibility and efficiency through the proposal of original architectures that break the limits of the existing ones. This exploration and study have been conducted at three levels: interconnect, processing, and memory levels. At interconnect level, we have explored the use of memristive devices to allow high degree of flexibility based on programmable interconnects. This allows to propose the first memristor-based reconfigurable fast Fourier transform architecture, namely mrFFT. Memristors are inserted as reconfigurable switches at the level of interconnects in order to establish flexible on-chip routing. At processing level, we have explored the use of memristive devices and their integration with CMOS technologies for combinational logic design. Such hybrid memristor-CMOS designs exploit the high integration density of memristors in order to improve the performance of digital designs, and particularly arithmetic logic units. At memory level, we have explored new in-memory computing approaches and proposed a novel logic design style, namely Memristor Overwrite Logic (MOL), associated with an original MOL-based computational memory. The proposed approach allows efficient combination of storage and processing in order to bypass the memory wall problem and thus to improve the computational efficiency. The proposed approach has been applied in three real application case studies for the sake of validation and performance evaluation.

Mots-clés: Memristor ; In-memory computation ; Crossbar array ; Logic design ; Non-volatile memory

Le jury est composé de :

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